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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,712	09/30/2003	Ken Drottar	884.A81US1	2957

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EXAMINER	
WHITE, DYLAN C	
ART UNIT	PAPER NUMBER
2819	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/676,712	DROTTAR ET AL.	
	Examiner	Art Unit	
	Dylan White	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

The Examiner acknowledges the common Assignee (Intel) between the cited prior art of Martin and the present Application, and the Applicants argument for exclusion of such art under 35 USC § 103(c). The rejection under 35 USC § 103(a) in view of martin has been withdrawn.

Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20, are rejected under 35 U.S.C. 103(a) as being unpatentable over Arcoleo et al. (US Pat. 5,864,506) in view of Marshall et al. (US Pat. 6,876,224).

Regarding claim 1, Arcoleo discloses a first circuit (transistors 603a-b) couple to an input port (601 @ Fig. 6) of the transmitter (Fig. 6), the first circuit including an port (601) and an output port (between transistors 603a-b) and no more than two transistors

(603a-b) including a first transistor (603a) having a source/drain directly connected to a source/drain of the second transistor (603b), the second transistor larger than the first transistor (col. 8, lines 20-26); and a second circuit (604a-b & 605a-b) including an input port (between transistors (604a-b) to the output port of the first circuit (between transistors 603a-b), the second circuit including an output port (between transistors 605a-b) coupled to the output port of the transmitter (602).

Arcoleo fails to teach where the first and second circuits are sized such that for an input signal the transmitter generates and output signal with a rise and fall time substantially equal to the input signal.

Marshall discloses a transmitter (Fig. 2) with a first (transistors 210 & 230) and second (transistors 208, 228, 206, & 226) where the first circuit is sized with respect to the second circuit such that for an input signal the transmitter generates an output signal having a rise-time and fall-time that are substantially equal at the output port of the transmitter (Fig. 1c, rise and fall time of waveform 130 is substantially equal), therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the transmitter disclosed by Arcoleo and the equal waveform taught by Marshall for impedance matching and improved signal quality.

Regarding claim 2, the combination discloses where the first circuit includes an inverter (Arcoleo, transistors 603a-b @ Fig. 6).

Regarding claim 3, the combination discloses where the inverter includes n-type MOSFET (Arcoleo, 603b @ Fig. 6) in series with a p-type MOSFET (603a).

Regarding claim 4, the combination discloses where the n-type MOSFET is larger than the P-type MOSFET (col.8, lines 20-26).

Regarding claim 5, the combination discloses where the n-type MOSFET is between about two and about three times larger than the P-type MOSFET (col. 8, lines 20-26). Furthermore the MPEP states (2144.04 IV. A)

> In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

Therefore, simply changing the size of the transistors does not change the operation of the circuit to give it patentable weight over the prior art.

Regarding claim 6, the combination discloses where the second circuit includes a plurality of driver circuits (Arcoleo, 604 & 605 @ Fig. 6).

Regarding claim 7, the combination discloses where each of the plurality of driver circuits (Arcoleo, Fig. 6) includes a p-type MOSFET connected in series with an N-type MOSFET (604a-b, 605a-b)

Regarding claim 8, the combination discloses where the P-type MOSFET is sized to source a first current (from V_{cc} 20) and the N-type MOSFET is sized so sink a second current (to GND 22) substantially equal to the first current (the transistors have to be sized in order to handle substantially equal first and second currents, if the transistors were too small they would burn out).

Regarding claim 9, the combination discloses where the second circuit (Arcoleo, 604a-b & 605a-b) is connected to an equalization control circuit (611).

Regarding claim 10, the combination discloses where the equalization control provides de-emphases (col. 9, lines 29-48).

Regarding claim 11, the combination discloses where the transmitter transmits at a signal level and the first circuit and the second circuit are coupled to a supply voltage potential (V_{cc}) having a value about twice the signal level (the transmit voltage will be lower than the supply voltage based on the physical size of transistors 604-607a. The combination between the value of the supply voltage and the physical size of the transistors can make the voltage supply about twice that of the transmission voltage).

Regarding claim 12, Arcoleo discloses receiving a first signal (at node 601 @ Fig. 6) at a first circuit (transistors 603a-b), the first circuit including an port (601) and an

output port (between transistors 603a-b) and no more than two transistors (603a-b) including a first transistor (603a) having a source/drain directly connected to a source/drain of the second transistor (603b), the second transistor larger than the first transistor (col. 8, lines 20-26); a second circuit (604a-b & 605a-b) coupled to the first circuit (Fig. 6), the second circuit including a plurality of P-type MOSFET's (604a, 605a), enabling the plurality of P-type MOSFET's to drive a transmission line (connected to node 602); and enabling less than the plurality of P-type MOSFET's (via control generator 611) to drive the transmission line.

Arcoleo fails to teach where the first and second circuits are sized such that for an input signal the transmitter generates and output signal with a rise and fall time substantially equal to the input signal.

Marshall discloses a transmitter (Fig. 2) with a first (transistors 210 & 230) and second (transistors 208, 228, 206, & 226) where the first circuit is sized with respect to the second circuit such that for an input signal the transmitter generates an output signal having a rise-time and fall-time that are substantially equal at the output port of the transmitter (Fig. 1c, rise and fall time of waveform 130 is substantially equal), therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the transmitter disclosed by Arcoleo and the equal waveform taught by Marshall for impedance matching and improved signal quality.

Regarding claim 13, the combination discloses receiving a signal at a first circuit (transistors 603a-b) includes receiving a digital signal (at node 601).

Regarding claim 14, the combination discloses enabling the plurality of P-type MOSFET's (603a, 604a, 605a) to drive a transmission line (at node 602) includes enabling the plurality of P-type MOSFET's substantially simultaneously (same gate signals).

Regarding claim 15, the combination discloses where enabling less than all of the P-type MOSFET's to drive the transmission line (Marshall, 200 @ Fig. 2) comprises enabling less than all of the p-type MOSFET's substantially simultaneously (don't have to enable all PMOS transistors).

Regarding claim 16, Arcoleo discloses a transmitter (Fig. 6) including a first circuit (transistors 603a-b) coupled to an input port (601) of the transmitter, the first circuit including an input port (601) and an output port (between transistors 603a-b) and no more than two transistors (603a-b) including a first transistor (603a) and a second transistor (603b), the first transistor having a source/drain directly coupled to a source/drain of the second transistor (Fig. 6) the second larger than the first transistor (col. 8, lines 20-26); and a second circuit (604a-b & 605a-b) coupled to the first circuit (Fig. 6) to an output port of the transmitter (602), the second circuit coupled to an equalization control circuit (611), where the equalization control provides de-emphasis (Fig. 6);

Arcoleo fails to directly disclose a receiver and a transmission line connecting the transmitter to the receiver. However, it is obvious that a receiver is required to receive the transmitted data, and that a transmission line would connect the two.

Marshall discloses a system (Marshall, Fig. 6) comprising components (602-610) where a transmitter and receiver are needed to communicate between the components of the system, and where bus lines (602) would constitute a group of transmission lines. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the transmitter disclosed by Arcoleo within the system taught by Marshall for impedance matching and improved signal quality.

Regarding claim 17, the combination discloses where the first circuit is an inverter (Arcoleo, 603a-b @ Fig. 6) having a P-type MOSFET (603a) and an N-type MOSFET (603b), the N-type MOSFET being between about two and about three times larger than the P-type MOSFET (col. 8, lines 20-26). Furthermore the MPEP states (2144.04 IV. A)

> In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

Therefore, simply changing the size of the transistors does not change the operation of the circuit to give it patentable weight over the prior art.

Regarding claim 18, the combination discloses where the second circuit (605a-b & 605a-b) includes a voltage driver (Arcoleo, Fig. 6).

Regarding claim 19, the combination discloses where the second circuit includes a controllable source impedance (Arcoleo, 606a, 607a @ Fig. 6).

Regarding claim 20, Arcoleo discloses a first circuit (transistors 603a-b) coupled to an input port (601) of the transmitter (Fig. 6); a second circuit (604a-b & 605a-b) including a second input port (between transistors 604a-b) coupled to an output port of the first circuit (between transistors 603a-b), the second circuit including a second circuit output port coupled to the output port of the transmitter (602).

Arcoleo fails to teach where the first and second circuits are sized such that for an input signal the transmitter generates and output signal with a rise and fall time substantially equal to the input signal and where a first and second processor transmit and receive signals.

Marshall discloses a transmitter (Fig. 2) with a first (transistors 210 & 230) and second (transistors 208, 228, 206, & 226) where the first circuit is sized with respect to the second circuit such that for an input signal the transmitter generates an output signal having a rise-time and fall-time that are substantially equal at the output port of the transmitter (Fig. 1c, rise and fall time of waveform 130 is substantially equal). Furthermore, Marshall discloses drivers embodied in a system (col. 5, lines 54-55) with a first processor (604 left) and a second processor (604 right) where the transmitter

(Fig. 2) can transmit to a receiver (not shown, but obvious) through transmission line (602), therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the transmitter disclosed by Arcoleo with the system taught by Marshall for impedance matching to a transmission line for improved signal quality.

Claims 21-23, are rejected under 35 U.S.C. 103(a) as being unpatentable over Arcoleo et al. (US Pat. 5,864,506) in view of Marshall et al. (US Pat. 6,876,224) in further view of Song (US Pat. 6,614,258).

Regarding claim 21, the combination of Arcoleo and Marshall disclose that of claim 20, but fail to disclose a specific type of processor.

Song discloses where a processor in a dynamic logic array can be a very long instruction word processor (VLIW, col. 9, line17), therefore, It would have been obvious to one of ordinary skill in the art at the time of invention to use the transmitter combination of Arcoleo and Marshall with the VLIW processor taught by Song for faster processing of more complex functions.

Regarding claim 22, where the second processor is a complex instruction set processor (CISC, Song, col. 9, line 16).

Regarding claim 23, the combination discloses an equalization control (Arcoleo, 611 @ Fig. 6) coupled to the second circuit (604a-b & 605a-b) to provide de-emphasis (Fig. 6).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dylan White whose telephone number is (571) 272-1406. The examiner can normally be reached on m-f 7:30- 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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03/15/07